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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,651	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/30/2004 has been entered.

Response to Amendment

2. This Office action is in respond to the amendment filed in 08/30/2004.

Specification

3. The disclosure is objected to because of the following informalities:

In [0016], "the interconnect 265 may include 8 differential pairs, 9 pairs for data, and 9 pairs for address and command." should be -- the interconnect 265 may include 18 differential pairs, 9 pairs for data, and 9 pairs for address and command.--

Appropriate correction is required.

Claim Objections

4. Claim 1 is objected to because of the following informalities:

Claim 1 lines 4-5, "whether there is a cache hit from the array of tage address storage locations" should be -- whether there is a cache hit from the array of tag address storage locations--

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,178 hereinafter Stracovsky) in view of Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

Regarding claim 1, Stracovsky disclosures a memory controller, i.e., universal controller (104, figure 1b), comprising an array of tag address storage locations (114, figure 1b), and a command sequencer and serializer unit coupled to the array of tag address storage locations (figure 1b) to receive information regarding whether there is a cache hit from the array of tag address storage locations (col. 7 line 39 through col. 8 line 2), the command sequencer and serializer unit to control the data cache located on the memory module by delivering a plurality of commands over a plurality of command and address lines, i.e., buses (106-1 – 106-3), the commands sequentially delivered over a plurality of transfer periods of a memory access

transaction and each command being delivered within one of the transfer periods, the plurality of commands including an activate command and a cache fetch command, the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality of transfer periods, i.e., processor(s) outputs a read request to the command bus 106-2 substantially simultaneously with a corresponding memory address request on the address bus 106-1, and both address request and command are received in the memory controller via a configurable system interface, the system interface convert the received system command and system address as a universal command, (i.e., read transaction), the universal command is partition into five data fields, (i.e., partition into a plurality of segments), which including an activate command (i.e., an activate data field 204, figure 2a) and a cache fetch command, (i.e., read/write data field (206 and 208)), in addition, Stracovsky disclosures the command sequencer is able to provide appropriate timing intervals between the command components of the universal command to provide a sequenced command (i.e., each command being delivered within one of the transfer periods, and the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality of transfer periods) and (col. 6 line 19 through col. 8 line 2), furthermore, Stracovsky disclosures the memory controller is able to generate a universal command that is based upon the sequence of operations required to perform the required request, such a page read operation, a previously open page must be closed, the new page activated, and the read operation performed, all of which are comprehended in the single universal command structure with appropriate timing (col. 9 line 16 through col. 10 line 34). Stracovsky differs from the claimed invention in not specifically teaches the command sequencer and serializer unit to control a data cache located on

a memory module using the received information. However, Saulsbury discloses a system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Stracovsky in having a data cache located on a memory module, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claims 2-6, Stracovsky teaches the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period and each of the activate and cache fetch command including memory module destination information during a first transfer period and row address information during each of the four transfer periods, wherein the cache fetch command includes way information delivered during the last transfer period and the plurality of commands each delivered over four transfer periods (col. 6 line 50 through col. 8 line 2 and col. 9 line 15 through col. 10 line 34).

Regarding claims 7-12, Stracovsky teaches the plurality of commands further including a read command and a read and pre-load command differing in format only in the information delivered during a last transfer period and differing in cache hit information delivered during last transfer period, wherein the read command and the read and preload command includes memory module destination during a first transfer period and column address information during each of the four transfer periods, and wherein the read and pre-load command includes way information

delivered during the last transfer period and the plurality of commands each delivered over four transfer periods (col. 6 line 50 through col. 8 line 2 and col. 9 line 15 through col. 10 line 34).

Regarding claim 13, Stracovsky discloses a memory module (108, figure 1a), a memory controller (104, figure 1b) component including an array of tag address storage locations (114, figure 1b), processor(s) outputs a read request to the command bus 106-2 substantially simultaneously with a corresponding memory address request on the address bus 106-1, and both address request and command are received in the memory controller via a configurable system interface, the system interface convert the received system command and system address as a universal command, (i.e., read transaction), the universal command is partition into five data fields, (i.e., partition into a plurality of segments), which including an activate command (i.e., an activate data field 204, figure 2a) and a cache fetch command, (i.e., read/write data field (206 and 208)), in addition, Stracovsky disclosures the command sequencer is able to provide appropriate timing intervals between the command components of the universal command to provide a sequenced command (i.e., each command being delivered within one of the transfer periods, and the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality of transfer periods) and (col. 6 line 19 through col. 8 line 2), furthermore, Stracovsky disclosures the memory controller is able to generate a universal command that is based upon the sequence of operations required to perform the required request, such a page read operation, a previously open page must be closed, the new page activated, and the read operation performed, all of which are comprehended in the single universal command structure with appropriate timing (col. 9 line 16 through col. 10 line 34). Stracovsky differs from the claimed invention in not specifically teaches the command sequencer

and serializer unit to control a data cache located on a memory module using the received information. Stracovsky differs from the claimed invention in not specifically teaches the memory modules comprising at least one memory device, and a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller component over a plurality of command lines of a memory bus. However, Saulsbury discloses a system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1), the data cache and memory bank is in respond to the requests generated by the memory controller via the plurality of buses (108, 110, 112, 114 and 106). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory modules of Stracovsky comprising at least one memory device, and a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller component over a plurality of command lines of a memory bus, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claims 14-18, the limitations of the claims are rejected as the same reasons set forth in claims 2-6.

Regarding claim 19, Stracovsky discloses a system comprising a processor (102, figure 1b), a universal controller (104, figure 1b) operated as a memory controller comprising an array of tag address storage locations (114, figure 1b), and a command sequence and serializer unit (116, figure 1b) coupled to the array of tag address storage location, and a memory module (108,

figure 1b) coupled to the memory controller via a memory bus, processor(s) outputs a read request to the command bus 106-2 substantially simultaneously with a corresponding memory address request on the address bus 106-1, and both address request and command are received in the memory controller via a configurable system interface, the system interface convert the received system command and system address as a universal command, (i.e., read transaction), the universal command is partition into five data fields, (i.e., partition into a plurality of segments), which including an activate command (i.e., an activate data field 204, figure 2a) and a cache fetch command, (i.e., read/write data field (206 and 208)), in addition, Stracovsky disclosures the command sequencer is able to provide appropriate timing intervals between the command components of the universal command to provide a sequenced command (i.e., each command being delivered within one of the transfer periods, and the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality of transfer periods) and (col. 6 line 19 through col. 8 line 2), furthermore, Stracovsky disclosures the memory controller is able to generate a universal command that is based upon the sequence of operations required to perform the required request, such a page read operation, a previously open page must be closed, the new page activated, and the read operation performed, all of which are comprehended in the single universal command structure with appropriate timing (col. 9 line 16 through col. 10 line 34). Stracovsky differs from the claimed invention in not specifically teaches the memory modules comprising at least one memory device, and a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller component over a plurality of command lines of a memory bus. However, Saulsbury discloses a system (100, figure 1) comprising a memory

controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1), the data cache and memory bank is in respond to the requests generated by the memory controller via the plurality of buses (108, 110, 112, 114 and 106). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory modules of Stracovsky comprising at least one memory device, and a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller component over a plurality of command lines of a memory bus, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claims 20-24, the limitations of the claims are rejected as the same reasons set forth in claims 2-6.

Regarding claim 25, Stracovsky disclosures a method comprising sequentially delivering during a plurality of transfer periods of a memory transaction information, i.e., read/write transaction, corresponding to both an activate command and a cache fetch command, i.e., read/write data command from a memory controller (104, figure 1b) to a memory module (108, figure 1b) over memory bus (220, figure 1b), the information being portioned into a plurality of segments, i.e., data fields, corresponding to the plurality of transfer periods and each segment being transmitted via one of the commands line within one of the plurality of transfer periods, and delivering from the memory controller to the memory module during a last transfer period of the plurality of transfer period associated with the memory access transaction information differentiating between an activate command and a cache fetch command, i.e., processor(s)

outputs a read request to the command bus 106-2 substantially simultaneously with a corresponding memory address request on the address bus 106-1, and both address request and command are received in the memory controller via a configurable system interface, the system interface convert the received system command and system address as a universal command, (i.e., read transaction), the universal command is partition into five data fields, (i.e., partition into a plurality of segments), which including an activate command (i.e., an activate data field 204, figure 2a) and a cache fetch command, (i.e., read/write data field (206 and 208)), in addition, Stracovsky disclosures the command sequencer is able to provide appropriate timing intervals between the command components of the universal command to provide a sequenced command (i.e., each command being delivered within one of the transfer periods, and the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality of transfer periods) and (col. 6 line 19 through col. 8 line 2), furthermore, Stracovsky disclosures the memory controller is able to generate a universal command that is based upon the sequence of operations required to perform the required request, such a page read operation, a previously open page must be closed, the new page activated, and the read operation performed, all of which are comprehended in the single universal command structure with appropriate timing (col. 9 line 16 through col. 10 line 34). Stracovsky differs from the claimed invention in not specifically teaches the commands from a memory controller to a memory moduel over a plurality of command lines of a memory bus. However, Saulsbury discloses a system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory

bank (118, figure 1), the data cache and memory bank is in respond to the requests generated by the memory controller via the plurality of buses (108, 110, 112, 114 and 106). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory modules of Stracovsky comprising at least one memory device, and a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller component over a plurality of command lines of a memory bus, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 26, Stracovsky discloses the method wherein delivering during a last transfer period information differentiating between an activate command and a cache fetch command includes delivering one of cache way and cache hit information (col. 6 line 50 through col. 8 line 32).

Regarding claim 27, the limitations of the claim are rejected as the same reasons set forth in claim 25.

Regarding claim 28, the limitations of the claim are rejected as the same reasons set forth in claim 26.

Response to Arguments

7. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tue-Fri 8:00 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo Li
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